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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,577	12/04/2003	Chen-Jung Tsai	0941-0874P	5109

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,577	TSAI ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/12/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/21/06 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5, 10, 18 and 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Foster et al. (U.S. Patent No. 6,603,072).

In re claims 1, 5, 10, 18 and 21, Foster (esp. Fig. 2) discloses a dual chips stacked packaging structure, comprising:

a first chip (lower 206), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (302), comprising a plurality of leads and a chip paddle (204) having a first adhering surface (at lower resin 212) and second adhering surface (at resin upper 212), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface (within the encapsulant) and an opposing wire non-connecting surface (outside of the encapsulant).

a second chip (upper 206), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bond pads, wherein the central area of the active surface of the first chip adheres to the first adhering surface of the chip paddle while an opposing central area of the opposing non-active surface of the second chip adheres to the second adhering surface of the chip paddle, and wherein the opposing central area of the opposing non-active surface of the second chip is opposite to the central area of the active surface of the second chip; and

a plurality of wires (308), wherein parts of the wires electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of the wires electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation (316) covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

In re claim 2, Foster discloses the device of claim 1, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive (212; column 4, lines 1-7).

In re claim 3, Foster discloses the device of claim 1, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (212; column 4, lines 1-7).

In re claim 4, Foster discloses the device of claim 1, wherein the wires are metal lines.

In re claim 6, Foster discloses the device of claim 5, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

In re claim 7, Foster discloses the device of claim 5, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive.

In re claim 8, Foster discloses the device of claim 5, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (212).

In re claim 9, Foster discloses the device of claim 5, wherein the wires are

metal lines.

In re claim 19, Foster discloses the device of claim 18, wherein the first and second chips adhere to either surface of the same parts of the chip paddle.

In re claim 20, Foster discloses the device of claim 18, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation. The limitation, "and the wire non-connecting surface ... to an exterior device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

In re claim 22, Foster discloses the device of claim 21, wherein an opposing central area of active surface of the first chip adheres to the first adhering surface of the chip paddle while the central area of the non-active surface of the second chip adheres to the second adhering surface of the chip paddle, and wherein the opposing central area of the active surface of the first chip is opposite to the central area of the opposing non-active surface of the first chip.

In re claim 23, Foster discloses the device of claim 21, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead (302) extending beyond the encapsulation, and the wire non-connecting surface of the leads remains exposed when the outer leads are attached to an exterior device.

Claim Rejections - 35 USC § 103

Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster as applied to claim 10 above, and further in view of Wu et al. (US 2003/0214048 Al).

In re claim 10, Foster (e.g., Fig. 2)discloses a dual chips stacked packaging structure, comprising:

a first chip (upper 206), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (302), comprising a plurality of leads and a chip paddle (204) having a first adhering surface (at resin 212) and second adhering surface (at resin 212), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface (within the encapsulant) and an opposing wire non-connecting surface (outside of the encapsulant).

a second chip (upper 206), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (308), wherein parts of the wires electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of the wires electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation (218) covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

Foster does not expressly disclose the non-active surface of the first chip being exposed from the encapsulant. Wu (esp. Fig. 6) discloses the non-active surface (351) of a first chip (35) being exposed from the encapsulant. It would have been obvious for one skilled in the art at the time of the invention to expose the first chip of Foster as disclosed by Wu for the purpose, for example, of improving the heat-dissipating efficiency of the semiconductor device package structure (Wu; section [0029], lines 10-14).

The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device,

In re claim 11, Foster in view of Wu discloses the device of claim 10, wherein each lead (18) further comprises an inner lead (20) covered by the encapsulation and outer lead extending beyond the encapsulation.

In re claim 12, Foster in view of Wu discloses the device of claim 10, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[3].

In re claim 13, Foster in view of Wu discloses the device of claim 10, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 14, Foster in view of Wu discloses the device of claim 10, wherein the wires are metal lines.

In re claim 15, Foster in view of Wu discloses the device of claim 11, wherein the non-active surface of the first chip remains exposed.

The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

In re claim 16, Foster in view of Wu discloses the device of claim 11, wherein the wire non-connecting surface of the leads remains exposed. The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

In re claim 17, Foster in view of Wu discloses the device of claim 10, wherein the first and second chips adhering to either surface of the same parts of the chip paddle.

Response to Arguments

Applicant's arguments and response of 02/21/06 were sufficient to overcome the rejection based on Shim (US 2004/0061202 A1). However, the

new issues raised in the claims warranted a new search and the new Non-Final Rejection above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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